In the Claims:

1. (Currently Amended) An integrated semiconductor structure, having

~~———~~a substrate ~~(1)~~,

~~———~~at least one semiconductor element ~~(2)~~ located on the substrate ~~(1)~~,

~~———~~a pad metal ~~(3)~~ having a surface ~~(F)~~,

~~———~~a multiplicity of metal layers ~~(4.x)~~ which are located between the pad metal ~~(3)~~ and the substrate ~~(1)~~, and

~~———~~a multiplicity of insulation layers ~~(5.y)~~, which separate the metal layers ~~(4.x)~~ from one another,

~~———~~the pad metal ~~(3)~~ extending at least over part of the at least one semiconductor element ~~(2)~~,

wherein, below the surface ~~(F)~~ of the pad metal ~~(3)~~, at least the top two metal layers ~~(4.x, 4.x-1)~~ have a structure which in each case at least includes two adjacent interconnects,

at least below the surface of the pad metal, the interconnects of the top two metal layers have a multiplicity of apertures, and

the interconnects of the top two metal layers are arranged in such a manner with respect to one another that the apertures in the top interconnects are offset with respect to the apertures in the interconnects below. ~~(4.x.z, 4.x-1.z)~~

2. (Currently Amended) The integrated semiconductor structure as claimed in the preceding claim 1, wherein the number ~~z~~ of the interconnects ~~(4.x.z)~~ of a metal layer ~~(4.x)~~, beneath the surface ~~(F)~~ of the pad metal ~~(3)~~, is between 2 and 6.

3. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 1 to 2~~claim 1, wherein the interconnects ~~(4.x.z)~~ within a metal layer ~~(4.x)~~ are electrically insulated from one another.

4. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 1 to 3~~claim 1, wherein the interconnects ~~(4.x.z)~~ within a metal layer ~~(4.x)~~ are electrically connected to one another.

5. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 1 to 4~~claim 1, wherein the interconnects ~~(4.x.z)~~ within a metal layer ~~(4.x)~~ have a width ~~(B)~~ and are at a spacing ~~(A)~~ from one another, the ratio between the width ~~(B)~~ and the spacing ~~(A)~~ being between 3 and 20.

6. (Currently Amended) The integrated semiconductor structure as claimed in ~~the preceding~~ claim 5, wherein the ratio between the width ~~(B)~~ and the spacing ~~(A)~~ is 10.

7. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 1 to 6~~claim 1, wherein, at least below the surface ~~(F)~~ of the pad metal ~~(3)~~, there is a multiplicity of vias ~~(6)~~ which electrically connect the interconnects ~~(4.x.z)~~ of the top metal layer ~~(4.x)~~ to the interconnects ~~(4.x-1.z)~~ of the metal layer ~~(4.x-1)~~ below the top metal layer~~it~~, the vias ~~(6)~~ penetrating through the insulation layer between the top metal layer and the metal layer below the top metal layer ~~(5.y-1)~~.

8. (Cancelled)

9. (Currently Amended) The integrated semiconductor structure as claimed in ~~the preceding claim 8~~claim 1, wherein, at least below the surface ~~(F)~~ of the pad metal ~~(3)~~, the apertures ~~(7.x, 7.x-1)~~ have a total area of between 5% and 30% of the total area of the interconnects ~~(4.x.z, 4.x-1.z)~~.

10. (Currently Amended) The integrated semiconductor structure as claimed in ~~the preceding~~ claim 9, wherein the apertures ~~(7.x, 7.x-1)~~ have a total area of 20% of the total area of the interconnects ~~(4.x.z, 4.x-1.z)~~.

11. (Cancelled)

12. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 8 to 11~~claim 1, wherein the interconnects ~~(4.x.z)~~ of the top metal layer ~~(4.x)~~ lie approximately congruently above the interconnects ~~(4.x-1.z)~~ of the metal layer ~~(4.x-1)~~ below.

13. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 8 to 12~~claim 1, wherein the interconnects ~~(4.x.z)~~ of the top metal layer ~~(4.x)~~ are offset with respect to the interconnects ~~(4.x-1.z)~~ of the metal layer ~~(4.x-1)~~ below.

14. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 1 to 13~~claim 1, wherein the metal layers ~~(4.x)~~, at least for the most part, are made from a sufficiently hard metal.

15. (Currently Amended) The integrated semiconductor structure as claimed in ~~the preceding~~ claim 14, wherein the metal contains aluminum, copper, tungsten, molybdenum, silver, gold, platinum or alloys thereof.

16. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 1 to 15~~claim 1, wherein the surface ~~(F)~~ of the pad metal ~~(3)~~ covers a region which, within a metal layer ~~(4.x)~~, comprises at least 50% metal.

17. (Currently Amended) The integrated semiconductor structure as claimed in ~~the preceding~~ claim 16, wherein the metal is distributed uniformly beneath the surface ~~(F)~~ of the pad metal ~~(3)~~.

18. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 1 to 17~~claim 1, wherein a top insulation layer ~~(5.y)~~ is provided between the pad metal ~~(3)~~ and the top metal layer ~~(4.x)~~, the top insulation layer ~~(5.y)~~ having a first thickness ~~(D1)~~ and the top metal layer ~~(4.x)~~ having a second thickness ~~(D2)~~, and the ratio between the two thicknesses ~~(D1, D2)~~ being between 1 and 5.

19. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 1 to 18~~claim 1, wherein a top insulation

layer ~~(5.y)~~ is provided between the pad metal ~~(3)~~ and the top metal layer ~~(4.x)~~, the top insulation layer ~~(5.y)~~ having a first thickness ~~(D1)~~ and the pad metal ~~(3)~~ having a ~~further~~ second thickness ~~(D3)~~, and the ratio between the two thicknesses ~~(D1, D3)~~ being between 0.5 and 3.

20. (Currently Amended) The integrated semiconductor structure as claimed in ~~one of the preceding claims 1 to 19~~claim 1, wherein the number ~~x~~ of the metal layers ~~(4.x)~~ is between 3 and 11.